Specification

TFT-LCD module

Module(型号)：	392-B4042
Customer（客户）：	
Customer P/N（客户型号）：	

Approved by（批准）：	
Qualified（合格）：	**Unqualified（不合格）：**

PREPARED	CHECKED	APPROVED

Revision history

Date	Version	Revise record	Page	Design by
2020-11-11	A0	Original version		

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1. Introduction And General Specifications

1.1 Introduction

392-B4042 is a color active matrix TFT LCD Q-panel using amorphous silicon TFT „s(Thin Film Transistors) as an active switching devices. This Q-panel has a 3.92 inchdiagonallymeasured active area with Z2 resolutions (320 horizontal by 320 verticalpixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged invertical stripe and this Q-panel can display 16.7Mcolors.

1.2 General specification

Parameter	Value	Unit
Size	3.92” inch	
Module outline (W x HxD)	76.72X74.86X2.1	
Active area (WxH)	71.13X69.82	
Display Resolution	320X320	pixels
Pixel Arrangement	RGB Vertical stripe	-
Display colors	16.7M	COLORS
Display Mode	Normally Black	
Interface Type	MCU/SPI	-
Power Supply Voltage	2.8/3.2	V
Back-light	White LED*10	pcs
Driver IC	ST7796	

1.3 Absolute Maximum Ratings

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Environment Absolute Maximum Ratings> [Ta =25±2 ℃]

Parameter	Symbol	Min.	Max.	Unit	Remarks
Operating Temperature	T_{OP}	-20	70	℃	
Storage Temperature	T_{ST}	-30	80	℃	

Note:

1. These range above is maximum value not the actual operating temperature . Actual Operating temperature is no more than 40℃ and temperature refers to the LCM surface temperature ;
2. BOE is not responsible for product problems beyond the use conditions.

1.4 Electrical Specifications

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
System Voltage	VDD	2.5	2.8	3.6	V	
Interface Operation Voltage	VDDI	1.65	1.8	3.3	V	
TFT Gate ON Voltage	VGH	10	12	14	V	
TFT Gate OFF Voltage	VGL	-14	-12	-10	V	
TFT Common Electrode Voltage	VCOM	-	-	-	V	
Max Voltage of Source	VOP	-	-	5.0	V	

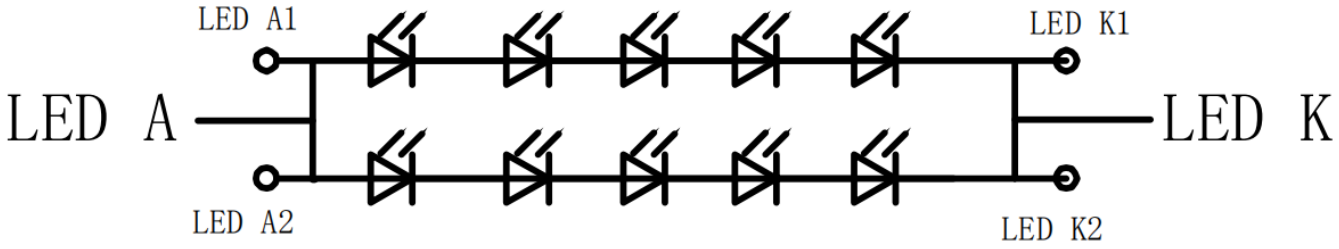
Notes :

1. VGH is TFT Gate operating voltage.
2. VGL is TFT Gate operating voltage. The low voltage level of VGL signal must be fluctuates with same phase as Vcom.
3. Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..
4. The value is just the reference value. The customer can optimize the setting value by the different D-IC

1.5 LCM And Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
LED forward voltage	VL	14.0	15.0	16.5	V	
LED forward current	IL	-	40	-	mA	
LCD forward current	IL	-	/	-	mA	
LED life time	-	-	-	-	Hr	
LED Luminance	Lv				cd/㎡	
LCM Luminance	Lv				cd/㎡	

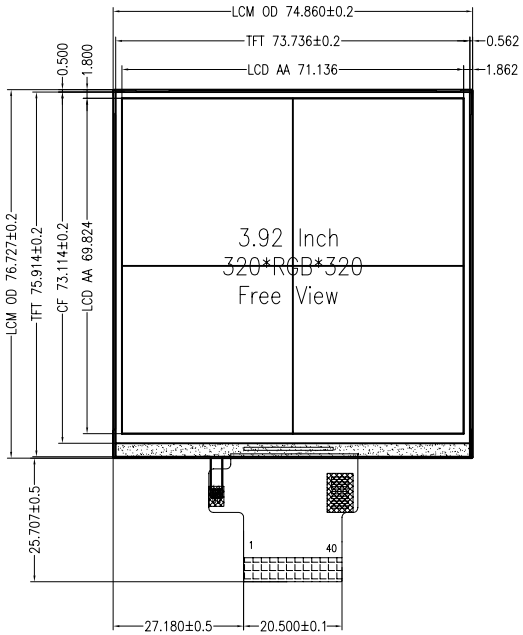
Note 1: The “LED life time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and IL =40mA. The LED lifetime could be decreased if operating IL is lager than40 mA.
Note 2: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and IL =40mA. In the case of 10 pcs LED , VL=3.0*5=15.0V
Note 3: The LED driving condition is defined for each LED module (5 strings 2 and).

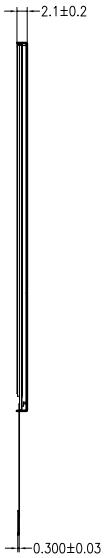


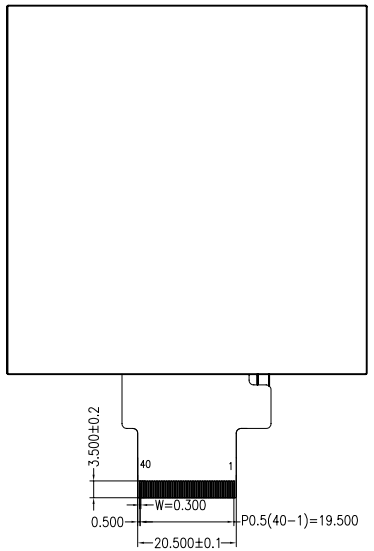
V=3.0V*5=15.0V

I =20mA*2=40mA

Reversion	Dispcription	Date	Signed







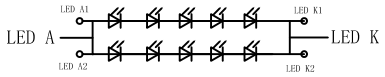
FPC INTERFACE

1	LEDK
2	LEDA
3	GND
4	VCC
5	IOVCC
6	GND
7	RESET
8	CS
9	RS
10	WR
11	RD
12	GND
13	IM0
14	IM1
15	IM2
16	SDO
17	SDA
18	GND
19	DB0
20	DB1
21	DB2
22	DB3
23	DB4
24	DB5
25	DB6
26	DB7
27	DB8
28	DB9
29	DB10
30	DB11
31	DB12
32	DB13
33	DB14
34	DB15
35	GND
36	CTP_VDD
37	CTP_CS
38	CTP_SCL
39	CTP_INT
40	CTP_RST

接口定义说明:
(IM2 IM1 IM0): 010 8080 16BIT(Data PIN DB0~DB15)
(IM2 IM1 IM0): 011 8080 8BIT(Data PIN DB0~DB7)
(IM2 IM1 IM0): 101 3SPI (Data PIN SDA SDO)
(IM2 IM1 IM0): 111 4SPI (Data PIN SDA SDO)

NOTES:

1. DISPLAY TYPE: TFT/Normally BLACK/transmisstive
2. OPERATING VOLTAGE: VCC:3.3V IOVCC:1.8V
3. OPERATING TEMPERATURE: −20°C~70°C
4. STORAGE TEMPERATURE: −30°C~80°C
5. VIEWING DIRECTION: Full VIEW
6. POLARIZER TYPE:
7. UNMARKED TOLERANCE: ±0.2



IF=40MA, VF=15V-15.5V

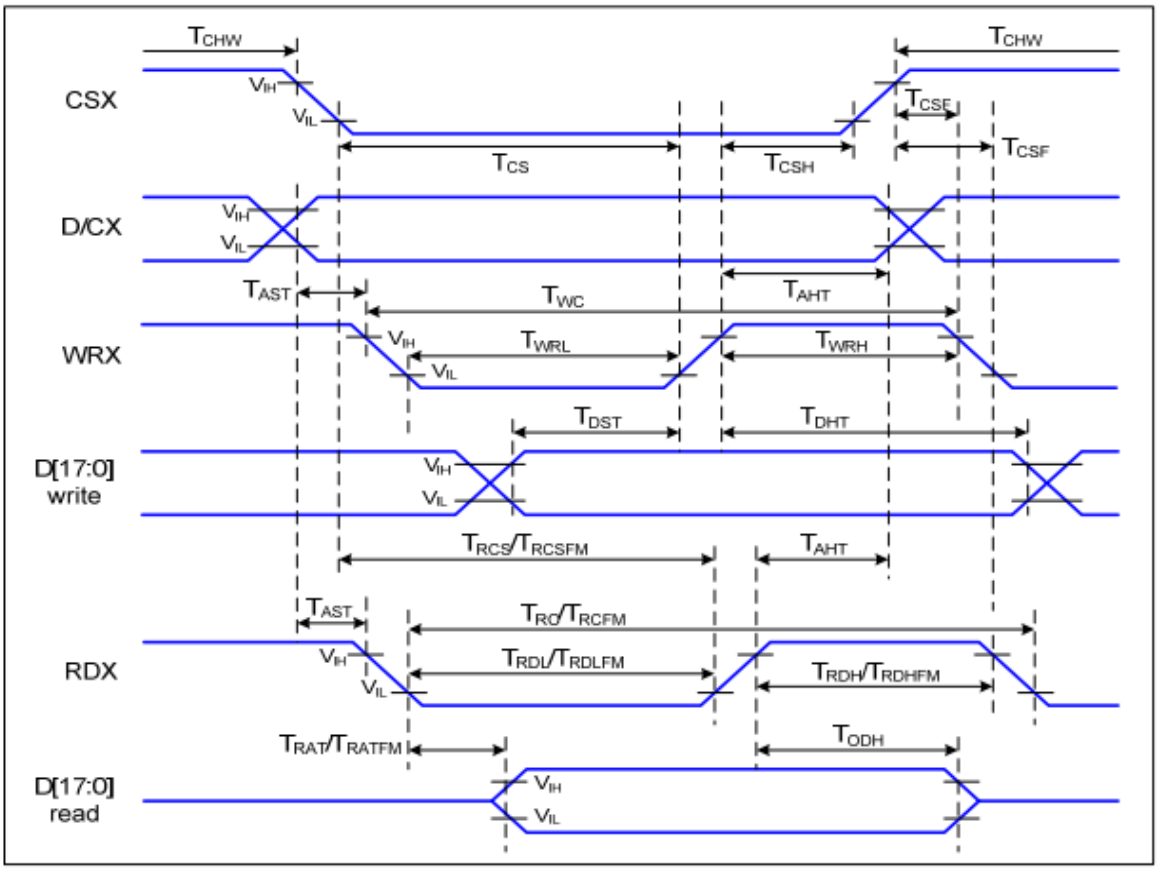
Custumer Ref.	Model No.		Drawing Title ---		Characteristics		
---	Approve		Material	Unmarked Tolerance	Unit	Scale	Page
Part No.	Checked			±0.2	mm	1:1	of
---	Draw		Date	14-9-18	Rev A0		
Drawing No.							

3.0 *INTERFACE PIN CONNECTIONS*

1	LEDK	LED CATHODE
2	KEDA	LED ANODE
3	GND	Ground
4	VCC	Power supply
5	IOVCC	Power supply
6	GND	Ground
7	RESET	Reset Signal ,Active Low
8	CS	Chipselectionpinlow:enablehigh:disable
9	RS	Displaydata/commandselectionpininparallelinterface
10	WR	WriteenableinMCUparallelinterface
11	RD	Readenablein8080MCUparallelinterface
12	GND	Ground
13	IM0	The MCU interface mode select
14	IM1	The MCU interface mode select
15	IM2	The MCU interface mode select
16	SDO	Display data/command selection pin in 4-line serial interface.
17	SDA	SPI interface in/output pin
18	GND	Ground
19	DB0	Data
20	DB1	Data
21	DB2	Data
22	DB3	Data
23	DB4	Data
24	DB5	Data
25	DB6	Data
26	DB7	Data
27	DB8	Data
28	DB9	Data
29	DB10	Data
30	DB11	Data
31	DB12	Data
32	DB13	Data
33	DB14	Data
34	DB15	Data
35	GND	Ground
36	CTP-VDD	Touch Power supply
37	CTP-CS	Touch IIC Data signal
38	CTP-SCL	Touch IIC Clock signal
39	CTP-INT	Touch Interrupt
40	CTP-RST	Touch Reset Signal

4. Characteristics

4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



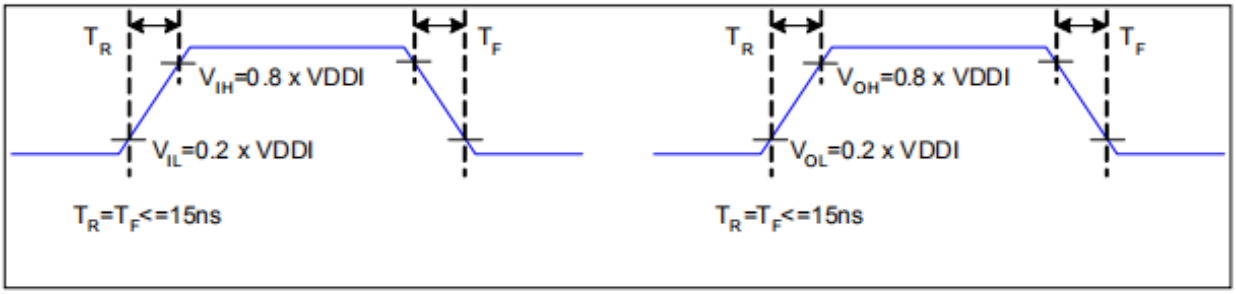
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

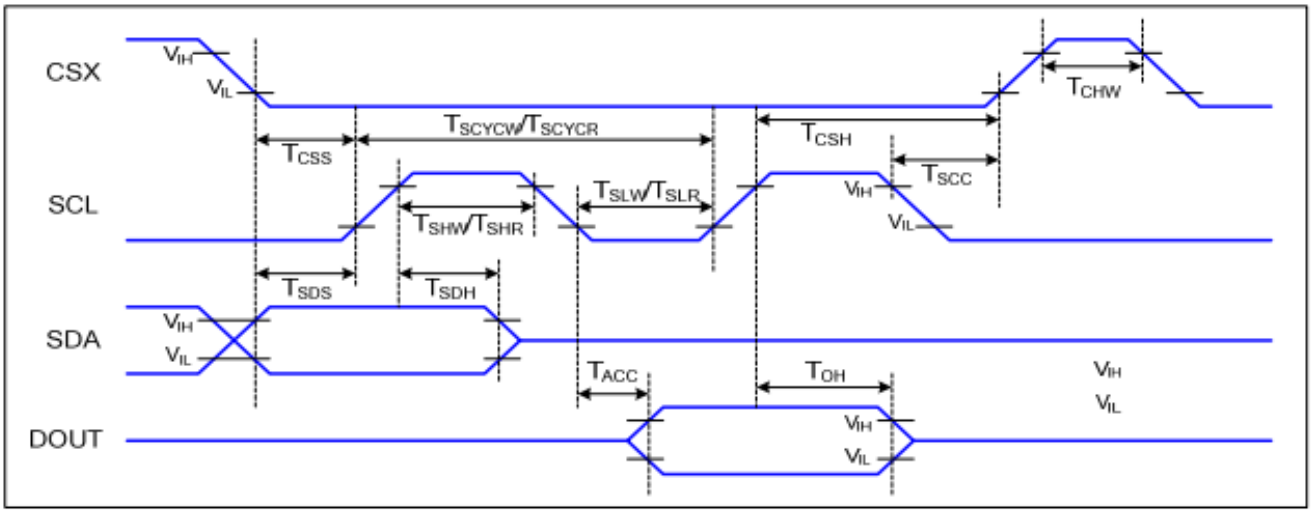
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

4.2. 3-SPI Serial Data Transfer Interface Characteristics:



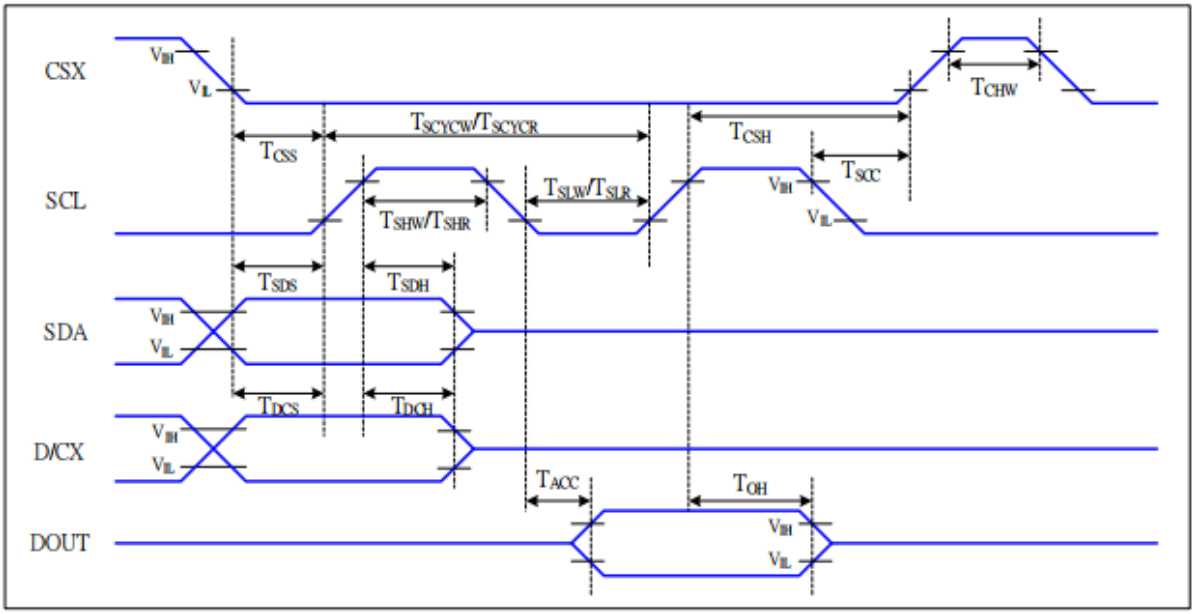
3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

4.3 4-SPI Serial Data Transfer Interface Characteristics:



4-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

4.4 POWER ON/OFF SEQUENCE：

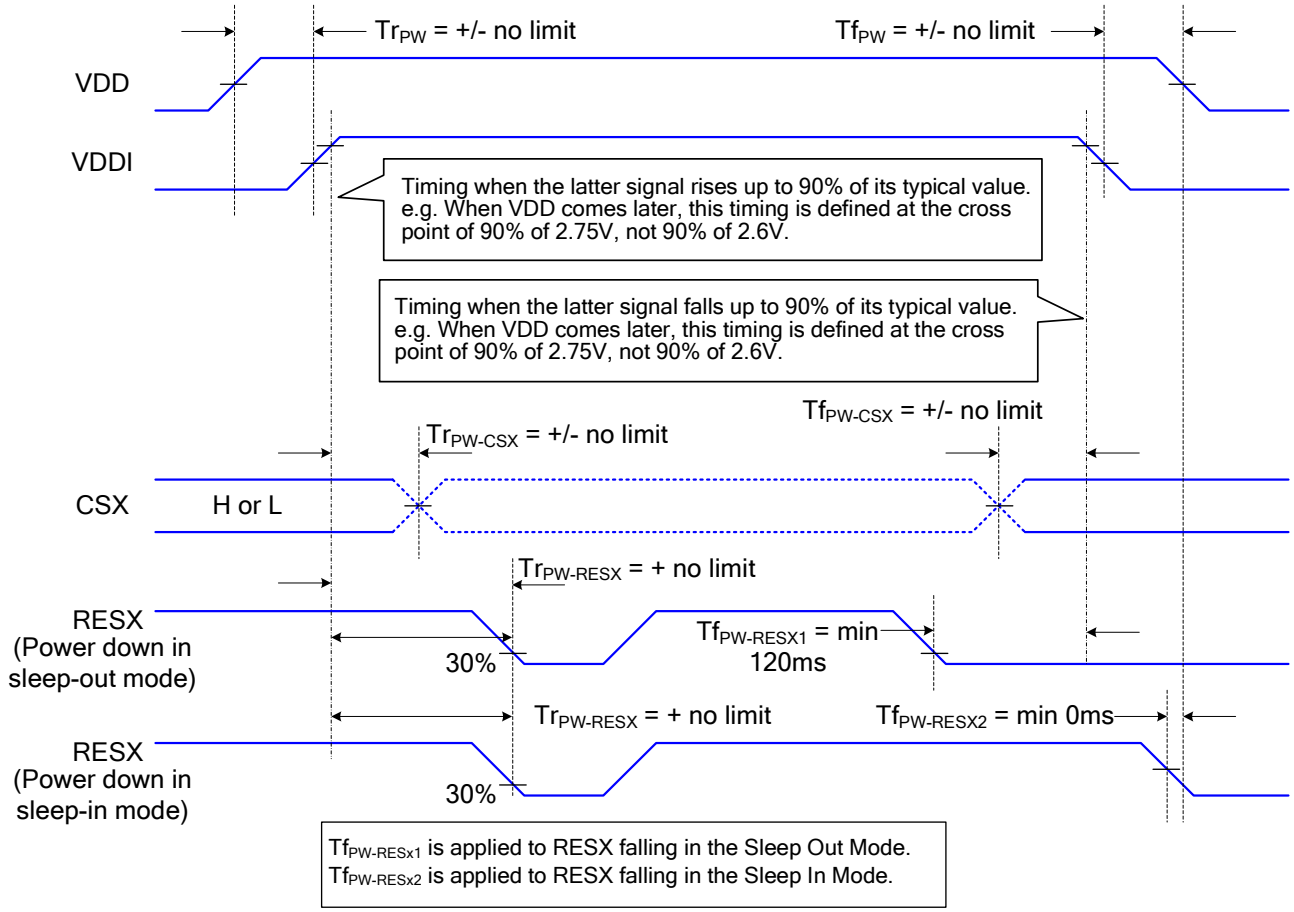
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



9.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5. *ELECTRO-OPTICAL CHARACTERISTICS*

The test of view angle range shall be measured in a dark room (ambient luminance ≤ 1lux and temperature = 25±2℃) with the equipment of Luminance meter system (Goniometer system and TOPCON CS2000/CA310) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θ Ø=90 (= θ12) as the 12 o'clock direction ("upward"), θ Ø=180 (= θ9) as the 9 o'clock direction ("left") and θ Ø=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The luminance, color and uniformity (etc) should be tested by CS2000/CA310. The backlight should be operating for 10 minutes prior to measurement. VDD shall be 3.3 ± 0.3V at 25°C. Optimum viewing angle direction is 6 'clock

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	75	85	-	Deg.	Note 1
		Θ_9		75	85	-	Deg.	
	Vertical	Θ_{12}		75	85	-	Deg.	
		Θ_6		75	85	-	Deg.	
Contrast ratio		CR	Θ = 0°	800	1000	-	-	Note 2
Transmittance		Tr		4.0	4.8	-	%	Note 3
Color Gamut	NTSC	CIE1931	Θ = 0°	55	60	-	%	Note 4 C Light
Reproduction of color	White	Wx	Θ = 0°	Typ -0.03	0.292	Typ +0.03	-	
		Wy			0.328		-	
Response Time		Tr+Td	Ta= 25° C Θ = 0°	-	25	35	ms	Note 5

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with APF and without CG.

4. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel and based on C Light

5. The electro-optical response time measurements shall be made as FIGURE 2. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

6. RELIABILITY

The Reliability test items and its conditions are shown in below.

<Table 6. Reliability test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 80 ℃, 240 hrs
2	Low temperature storage test	Ta = -30 ℃, 240 hrs
3	High temperature & high humidity (operation test)	Ta = 60 ℃, 90%RH, 240hrs
4	Low temperature operation test	Ta = -20 ℃, 240hrs
5	High temperature operation test	Ta = 70 ℃, 240hrs

Note :
After the reliability test, the product only guarantee function normally without any fatal defect (non-display, line defect, abormal display etc). All the cosmetic specification is judged before the reliablity test. The reliability test is based on ST7796U ;